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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,844	10/08/2004	Brent A. Anderson	BUR920040173US1	5843

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EXAMINER	
ERDEM, FAZLI	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
05/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,844	ANDERSON ET AL.	
	Examiner	Art Unit	
	Fazli Erdem	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *14-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-13* is/are rejected.

7)☒ Claim(s) *9, 19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11/30/2006 have been fully considered but they are not persuasive. Furukawa reference does teach a trench filled between a bulk region and an SOI region. In Fig. 7 of Furukawa et al., epitaxial semiconductor filled trench 20 is located between a bulk region that is located on the bottom left side of the trench 20 and an SOI region 14 on the upper right side of the epitaxy filled trench 20. Furthermore, looking at Fig. 11, epitaxy filled trench 20 is located between a bulk region on the bottom left side of trench 20 and a SOI/device region located on the upper right side of the trench 20.

1. Election restriction issued on 07/07/2006 has hereby been made final. Applicant argues the restriction on July 7, 2006, these arguments are not found to be persuasive because claims 14-18 recite specific manufacturing method steps that can be used to make another product. In the instant case in claim 14, with the specified method/manufacturing steps, regular type of sidewall spacer could be used instead of embedded type of sidewall spacer.

Allowable Subject Matter

2. Claims 9, 19 and 20 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. The following is a statement of reasons for the indication of allowable subject matter: Prior art failed to establish required crystal orientation.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (6,835,981) in view of Furukawa et al. (6,555,891).

Regarding Claims 1 and 2, Yamada et al. disclose a semiconductor chip which combines bulk and SOI regions and separates same with plural isolation regions where in Fig. 2 it is disclosed a semiconductor on insulator region on the right side with buried dielectric layer 22, a bulk semiconductor region on the left adjacent to the SOI region, a trench 47 disposed between the SOI region and bulk region. Yamada et al. fail to disclose the trench to be filled with epitaxial semiconductor material and the required sidewalls of the trench. However, Furukawa et al. disclose an SOI hybrid structure with selective epitaxial growth of silicon where the trench 20 is filled with epitaxial semiconductor and the required sidewalls 30.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required trench filling in Yamada et al. as taught by Furukawa et al. in order to have a semiconductor device with increased performance.

6. Claims 3-8 and 10-13 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (6,835,981) in view of Furukawa et al. (6,555,891) further in view of Yamada et al. (6,906,384)

Regarding Claims 3-8 and 10-13, Yamada et al.('981) disclose a semiconductor chip which combines bulk and SOI regions and separates same with plural isolation regions where in Fig. 2 it is disclosed a semiconductor on insulator region on the right side with buried dielectric layer 22, a bulk semiconductor region on the left adjacent to the SOI region, a trench 47 disposed between the SOI region and bulk region. Yamada et al. fail to disclose the trench to be filled with epitaxial semiconductor material with the required sidewalls of the trench and the required junction/doping configuration. However, Furukawa et al. disclose an SOI hybrid structure with selective epitaxial growth of silicon where the trench 20 is filled with epitaxial semiconductor and the required sidewalls 30. Furthermore, Yamada et al. ('384) disclose a semiconductor device having one of patterned SOI and SON region where in Figs, 2A, 3A and 4C the required junction/doping configuration is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required trench filling and the required junction/doping configuration in Yamada et al. as taught by Furukawa et al. and Yamada et al. ('384) in order to have a semiconductor device with increased performance.

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FE
April 26, 2007

SUE A. PURVIS
SUPERVISORY PATENT EXAMINER